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The New Era of Hybrid-Computing: Vector-Scalar to Vector-Digital Annealing, to Vector-Quantum Annealing

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Russian Supercomputing Days
September 27, 2021

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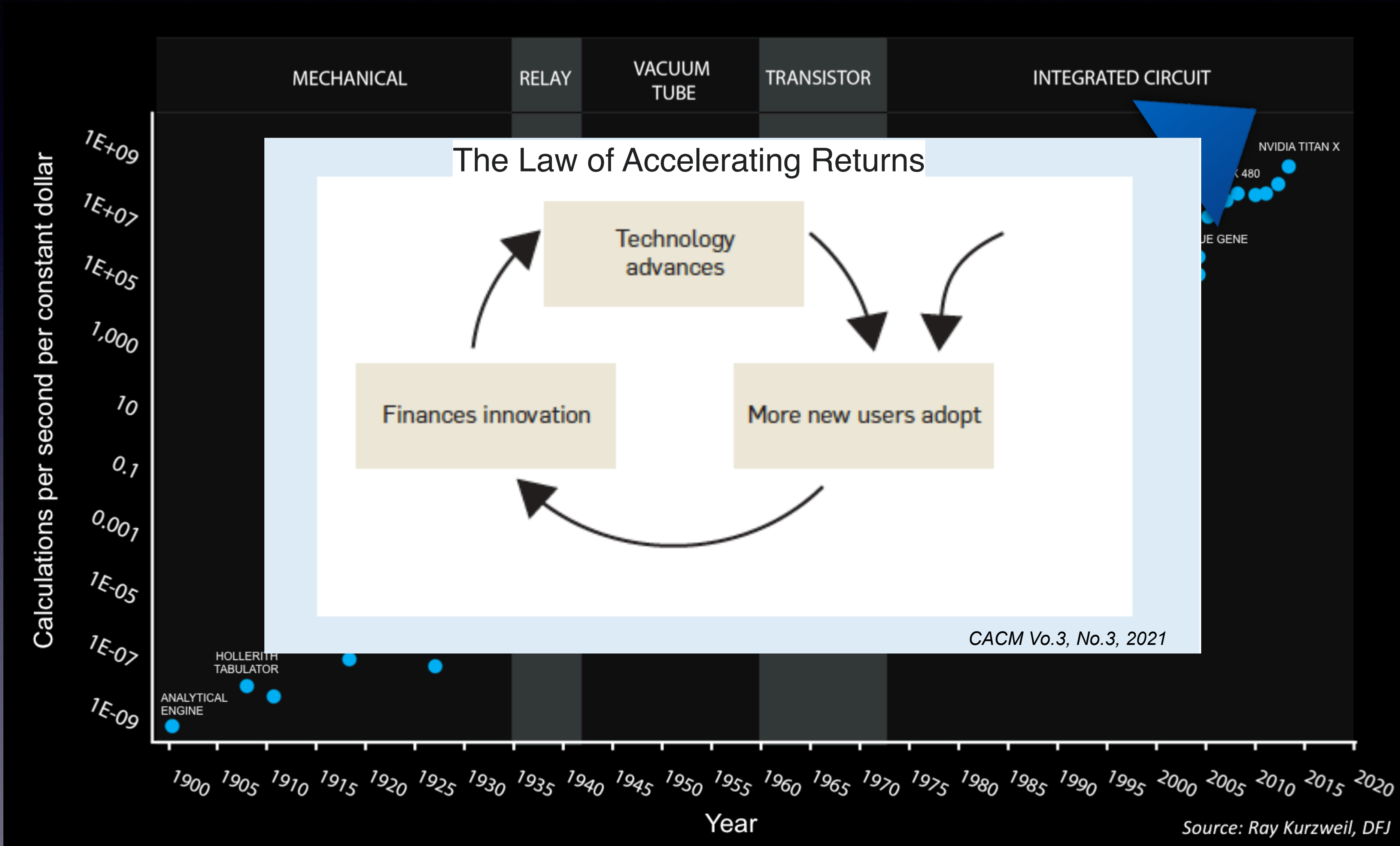
Today's Agenda

- ★ Background: Shifting from Pursuing General Pursue Monolithic Systems to Heterogeneous Computing Systems with a Wide-Variety of Domain-Specific Architectures (DSAs)
  - ✓ Facing the End of Moore's Law?
  - ✓ Maximize Sustained Performance and Power efficiency to select right architectures for different kernels/applications
  - ✓ Orchestrating different DSAs to realize general-purpose functionality, not depending only on a single architecture!
- ★ R&D of a Quantum Annealing-Classical HPC Hybrid Computing
  - Realize a Vector-Scalar and Quantum-Annealing Hybrid Simulation and Data Analysis Environment as a mix of DSAs
  - Provide a transparent interface to deductive and inductive computing platforms over the vector-scalar and quantum-annealing hybrid
  - ✓ Showcase application design and implementation of Data Analysis assisted by Digital and Quantum Annealing

120 Years of Moore's Law?



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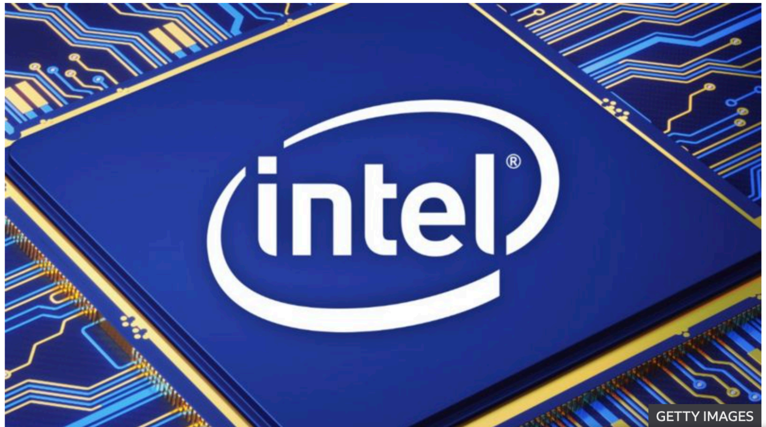
Tech

Intel's next-generation 7nm chips delayed until 2022

By Chris Fox
Technology reporter

24 July



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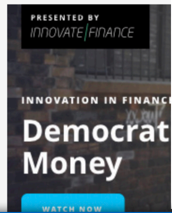

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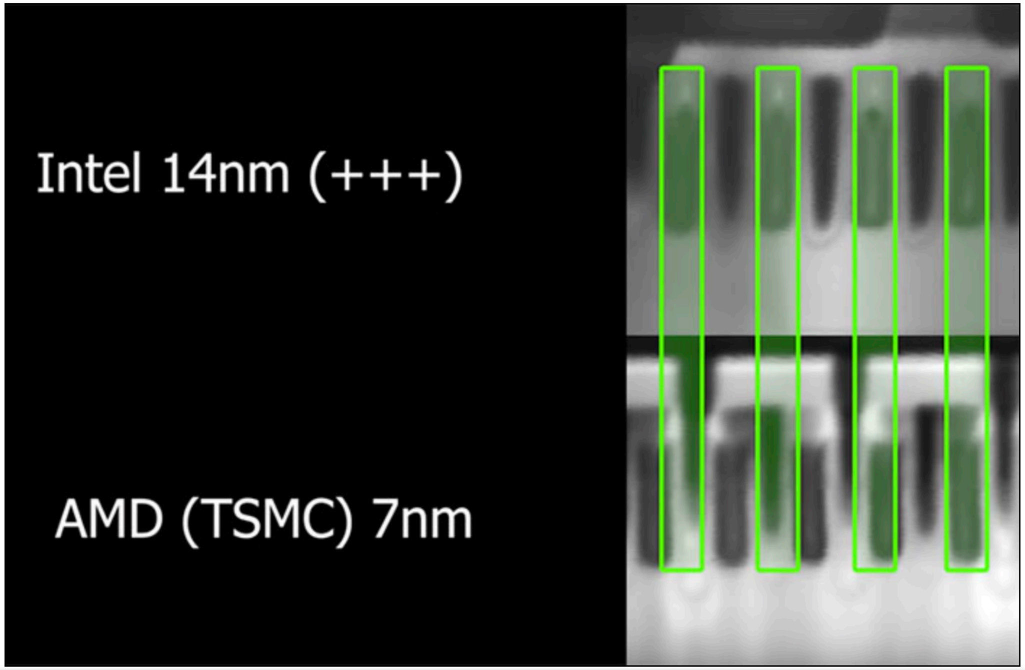
Wednesday, September 23rd 2020

Intel 14 nm Node Compared to TSMC's 7 nm Node Using Scanning Electron Microscope

by AleksandarK | Wednesday, 17:15 | Discuss (45 Comments)

Currently, Intel's best silicon manufacturing process available to desktop users is their 14 nm node, specifically the 14 nm+++ variant, which features several enhancements so it can achieve a higher frequencies and allow for faster gate switching. Compare that to AMD's best, a Ryzen 3000 series processor based on Zen 2 architecture, which is built on TSMC's 7 nm node, and you would think AMD is in clear advantage there. Well, it only sort of is. German hardware overclocker and hacker, der8auer, has decided to see how one production level silicon compares to another, and he put it to the test. He decided to use Intel's Core i9-10900K processor and compare it to AMD's Ryzen 9 3950X under a scanning electron microscope (SEM).



- ★Intel 14nm+++ and TSMC 7nm are very similar in physical scale
- ★Intel 10 nm and TSMC 7nm processes both produce dies with approx 90 million transistors per sq millimeter.

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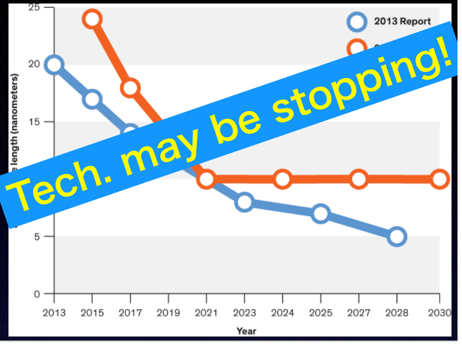
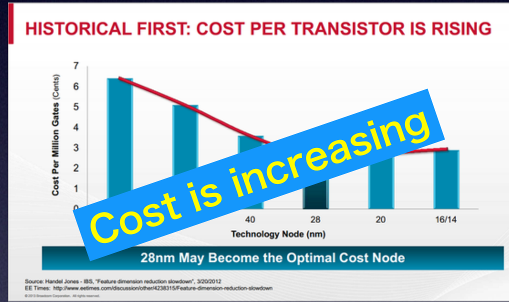
No More Moore's Law, No More One-Fits-All?!



- ✓ We are facing the end of Moore's law due to the physical limitations for miniaturization of transistors, and at the same time, the manufacturing cost is hard to reduce gradually,
  - ✓ Tech. is slowing, cost is increasing, and efficiency is lowering!



☆ Silicon is still fundamental constructing material for computing platforms just like plastic, steel and concrete for automobiles, buildings and home appliances.

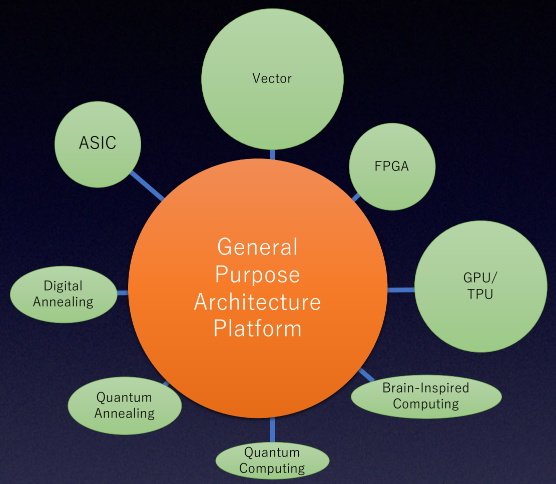
Use precious silicon budget (+ advanced device technologies) to effectively design mechanisms that can maximize the sustained performance of individual applications.

Rank	Name	Cores	Rmax (Tflop/s)	Rpeak (Tflop/s)	Rmax/Peak
1	Fugaku	7,299,072	415,530.00	513,854.70	80.87
2	Summit	2,414,592	148,600.00	200,794.90	74.01
3	Sierra	1,572,480	94,640.00	125,712.00	75.28
4	Sunway TaihuLight	10,649,600	93,014.60	125,435.90	80.87
[illegible]	Tianhe[illegible]	4,981,760	61,444.50	100,678.70	61.03
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible].54
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible].78
8	[illegible]a	[illegible]	[illegible]	[illegible]	[illegible].69

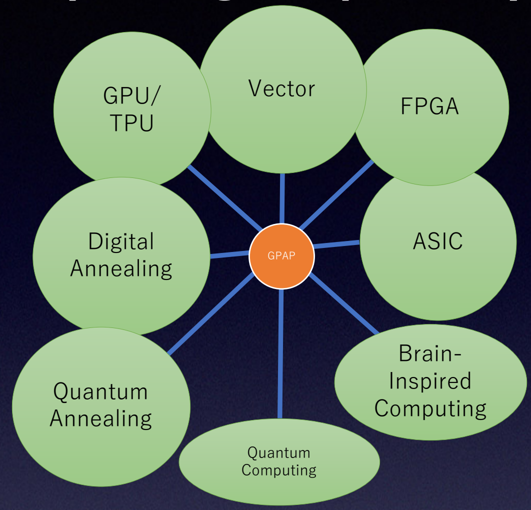
It's time to focus on Domain-Specific Architectures for computation-intensive, memory-intensive, I/O intensive, mixed-precision computing… etc applications to improve silicon/power efficiency, and their orchestration to satisfy the requirements from a wide variety of applications is required!

Hiroaki Kobayashi, Tohoku University

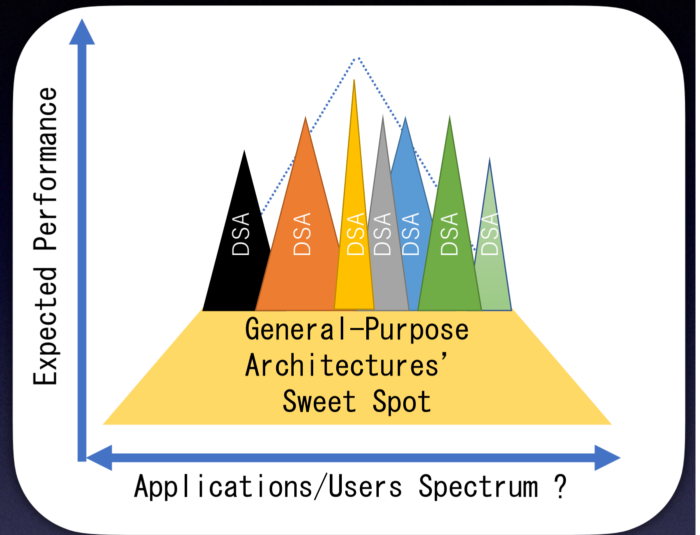
Moving to Hybrid Computing: Orchestrating a Wide Variety of DSAs to Realize General-Purpose Computing Capability!

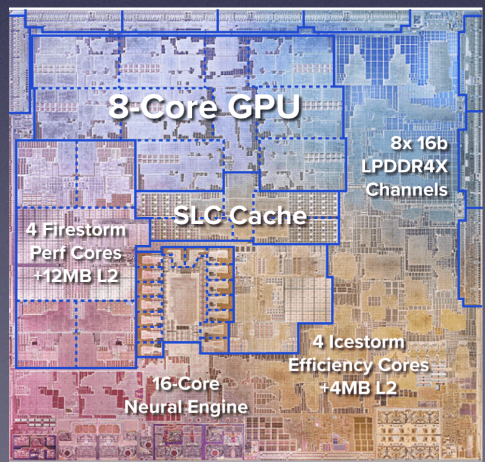


So far: General-Purpose Centric

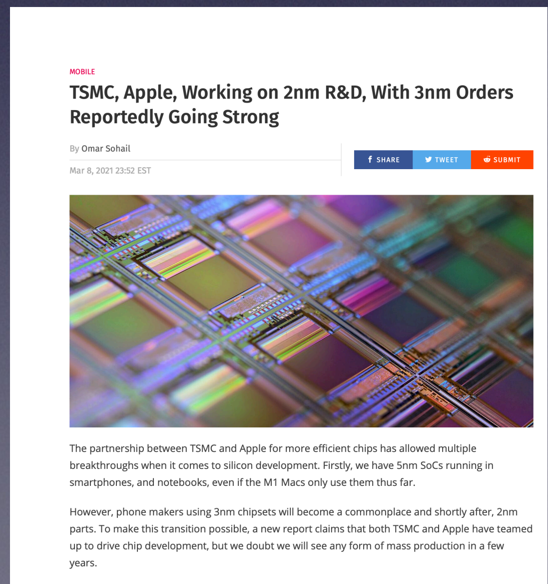


Future: DSA Hybrid





Apple M1 SoC
Source: Apple



MOBILE

TSMC, Apple, Working on 2nm R&D, With 3nm Orders Reportedly Going Strong

By Omar Sohail

Mar 8, 2021 23:52 EST

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The partnership between TSMC and Apple for more efficient chips has allowed multiple breakthroughs when it comes to silicon development. Firstly, we have 5nm SoCs running in smartphones, and notebooks, even if the M1 Macs only use them thus far.

However, phone makers using 3nm chipsets will become a commonplace and shortly after, 2nm parts. To make this transition possible, a new report claims that both TSMC and Apple have teamed up to drive chip development, but we doubt we will see any form of mass production in a few years.

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Toward Realization of Quantum Classical-HPC Hybrid Infrastructure

★ Tohoku University has established an interdisciplinary priority research institute, named Q-HPC, for Exploring Quantum Computing-Classical HPC Hybrid, in 2018

★ We start a new 5-year research program named “R&D of Quantum Annealing-Assisted HPC Infrastructure”, supported by MEXT, in collaboration with NEC and D-wave sys.

- ✓ provides transparent accesses to not only classical HPC resources but also Quantum Computing one in a unified fashion.
- ✓ Becomes an innovative infrastructure to develop next-generation applications in the fields of computational science, data sciences and their fusions

Innovative Applications in the fields of Computational Science, Data Science and their Fusion

QA-Assisted New Generation HPC infrastructure

Inductive Processing (for Data Science Apps.)

Tightly Coupling

Deductive Processing (for Computational Science Apps.)

QA Platform

QA-Assisted AI・ML Platform

X86-Assisted Vector Computing Platform

D-Wave Machines and/or equvs.?

SX-Aurora TSUBASA and its Successors?

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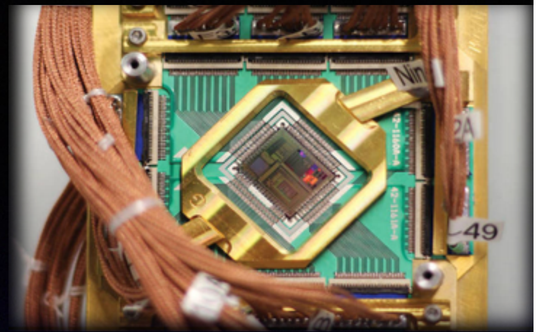
Quantum Computer: Emerging Domain Specific Architecture

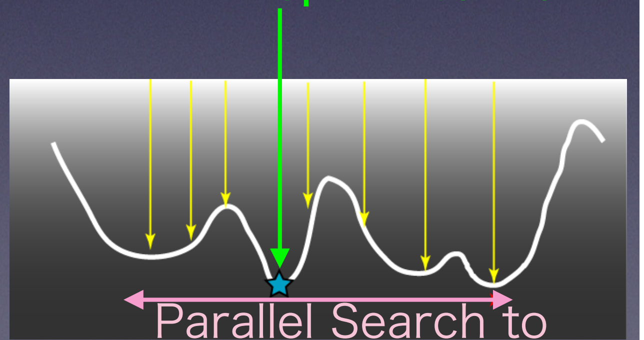


Source by D-Wave Sys.

Transverse magnetic field type quantum annealing Chip and System (D-Wave)

- ★ Quantum computing is drawing much attention recently as an emerging technology in the era of post-Moore
  - ✓ In particular, quantum annealing machines are commercialized by the D-wave systems, and their applications are developed world-widely.
    - ✓ Google, NASA, Volkswagen, Lockheed, Denso…
  - ✓ The base model named the Ising model to design and implement the D-wave machines has been proposed by Prof. Nishimori et al of Tokyo Inst. Tech. In 1998.
- ★ The quantum annealing is a metaheuristic for finding the global minimum of a given objective function over a given set of candidate solutions (candidate states), by a physical process named quantum fluctuations

Optimal solution

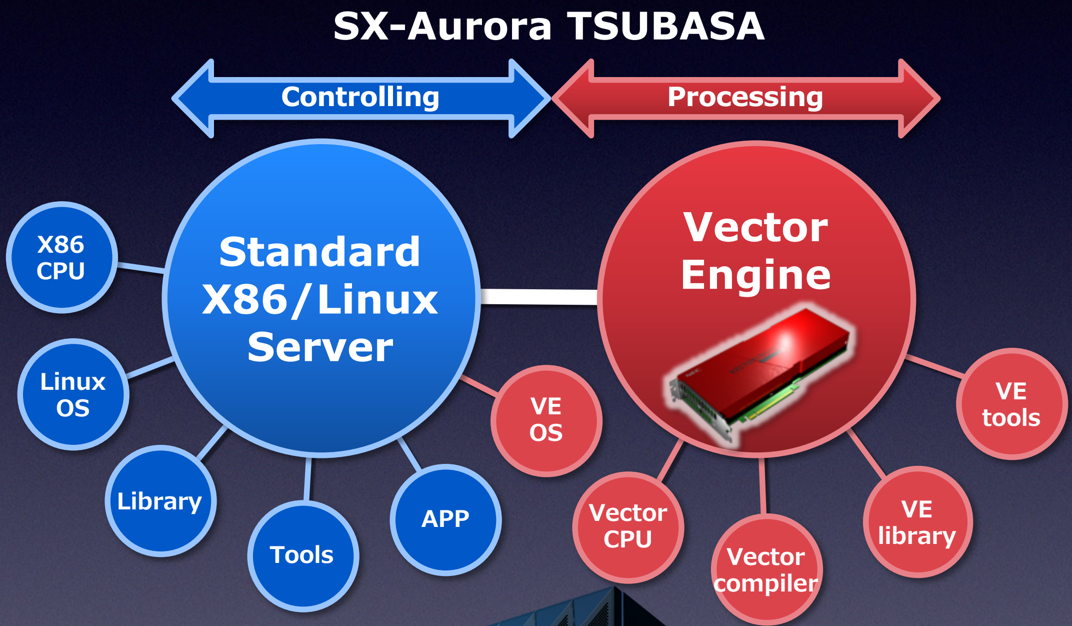


Parallel Search to reach optimal one by Quantum Fluctuation

An ideal solver for combinatorial problems!

Why Vector System: SX-Aurora-TSUBASA? ~Pursuing Balanced Architectures for High Sustained Performance~

Two types of balancing: computing performance and memory performance, and standardization and customization



Digital (Simulated) Annealing also Available!

Source:NEC

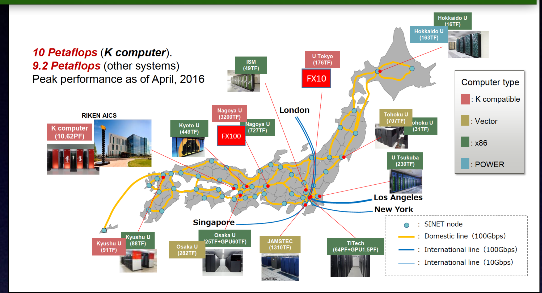
- ★ Customization for realization of the balanced vector architecture for memory-intensive apps
  - ✓ Highest Mem. BW
  - ✓ Largest Single Core Performance
- ★ Standardization for realization of the user-friendly environment and control-intensive apps.
  - ✓ x86 Linux Environment
  - ✓ New execution model centralized on vector computing

New Supercomputer System at Tohoku University

★ Start Servicing in Oct. 2020

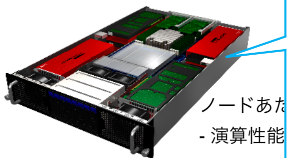
- Peak Performance of 1.8Pflop/s
- 20+ x performance-enhanced in 2022-23

HPCI for Nation-wide service

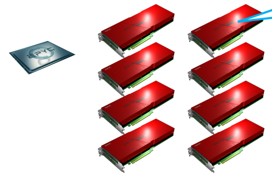


Vector Supercomputer SX-Aurora TSUBASA (2nd Gen VEs)

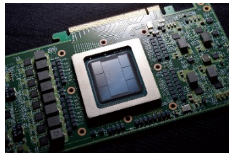
NEC SX-Aurora TSUBASA B4



AMD EPYC 7402P x 1
NEC Vector Engine Type 20B



NEC Vector Engine Cores x 8
HBM2 Memory Module x 6



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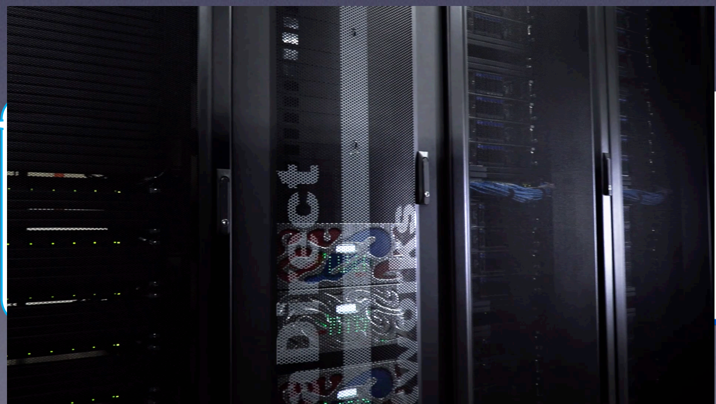
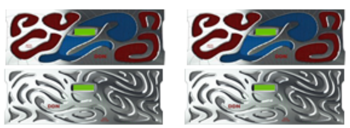
Interconnect Fabric (InfiniBand HDR)



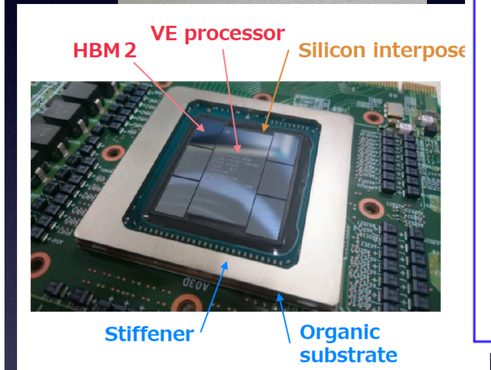
Storage 2PB
DDN SFA7990EX



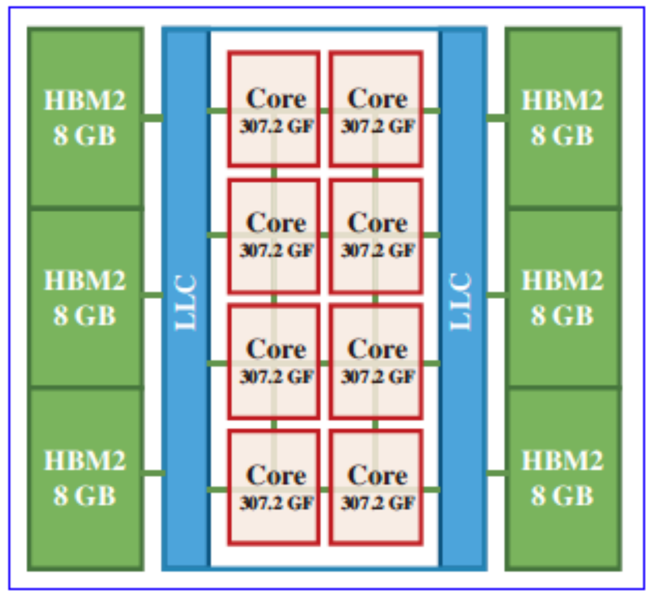
X86 Cluster System(AMD EPYC 7720)

Hiroaki Kobayashi, Tohoku University

Hardware Specification of SX-Aurora TSUBASA (2nd Gen in 2020)

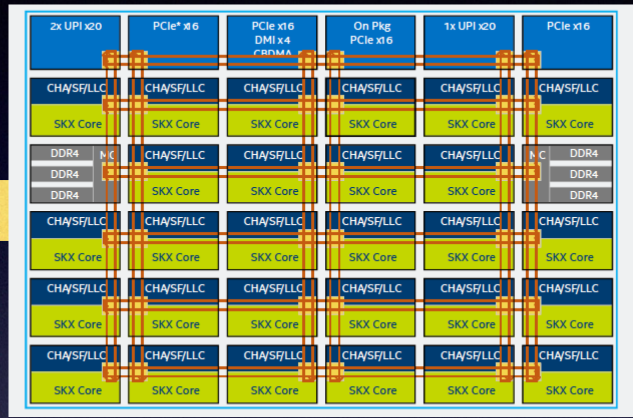


SX Vector Processor



PCIe

X86 Processor(Xeon)



Vector Engine (VE)	Type 20B
Frequency	1.6 GHz
Performance / Core	614 GF (SP), 307 GF (DP)
# cores	8
Performance / socket	4.91 TF (SP) 2.45 TF (DP)
Memory Subsystem	HBM2 8 GB x6
Memory Bandwidth	1.53 TB/s
Memory Capacity	48 GB

14% ↑

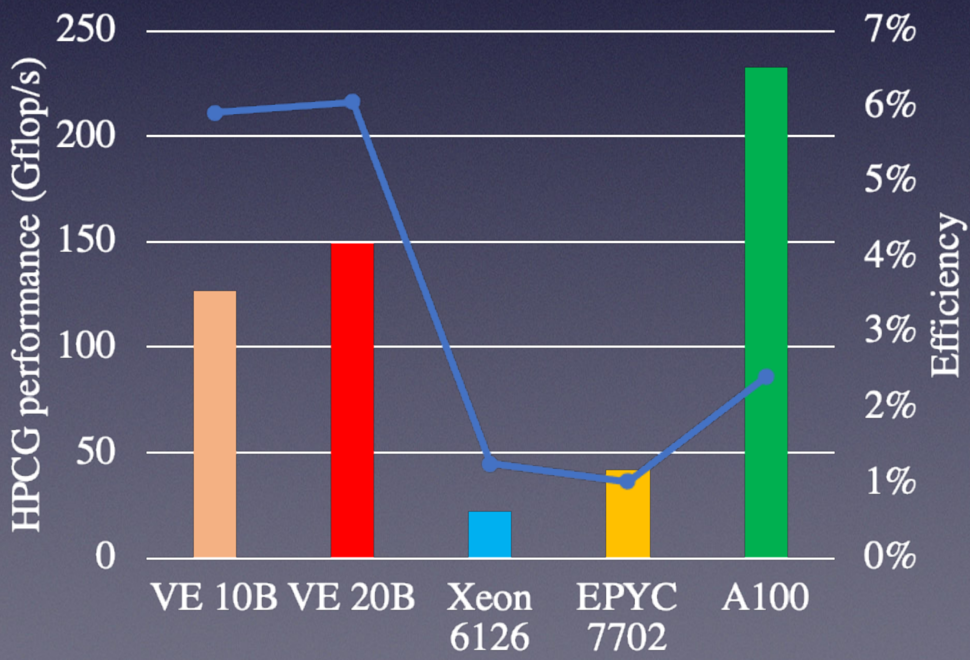
25% ↑

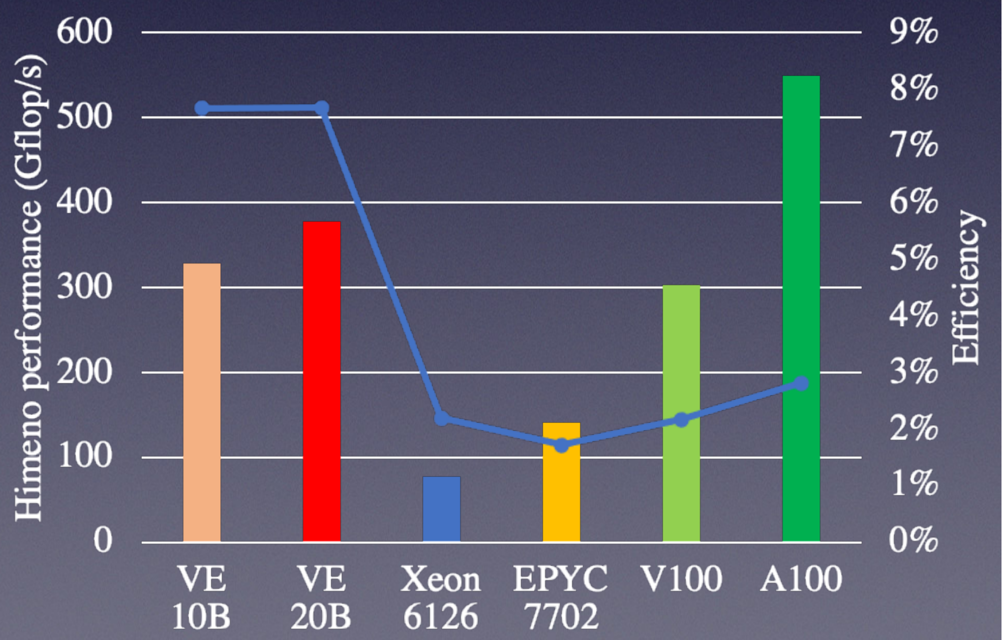
Vector Engine (VE)	Type 10B
Frequency	1.4GHz
Performance / Core	537.6 GF (SP), 268.8 GF (DP)
# cores	8
Performance / socket	4.30 TF (SP) 2.15 TF (DP)
Memory Subsystem	HBM2 8 GB x6
Memory Bandwidth	1.22 TB/s
Memory Capacity	48 GB

Hiroaki Kobayashi, Tohoku University

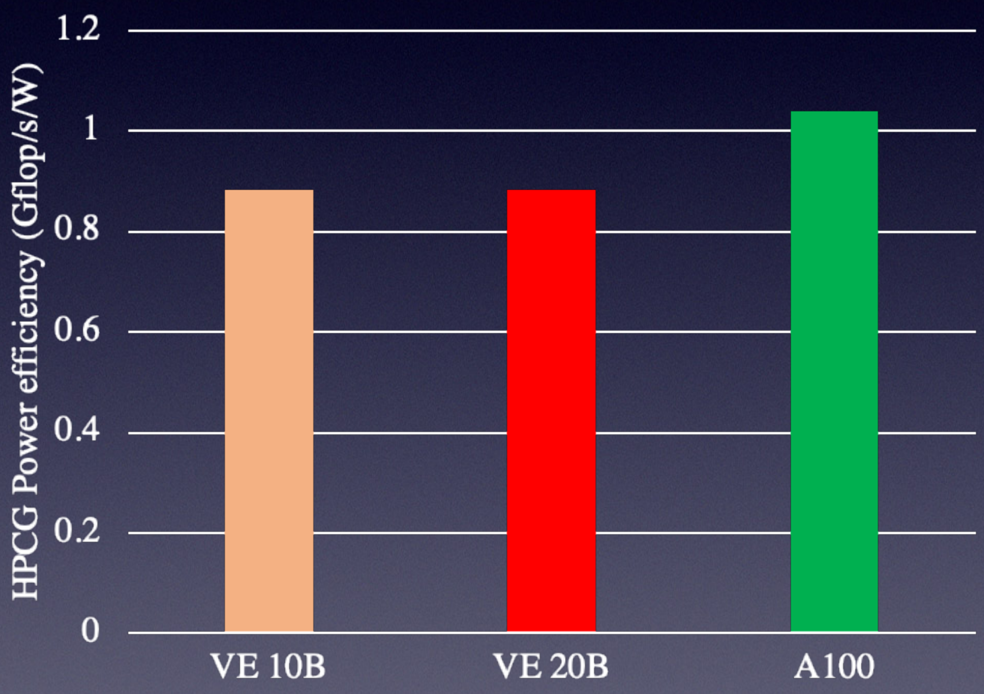
Potentials of SX-Aurora TSUBASA
Sustained Performance

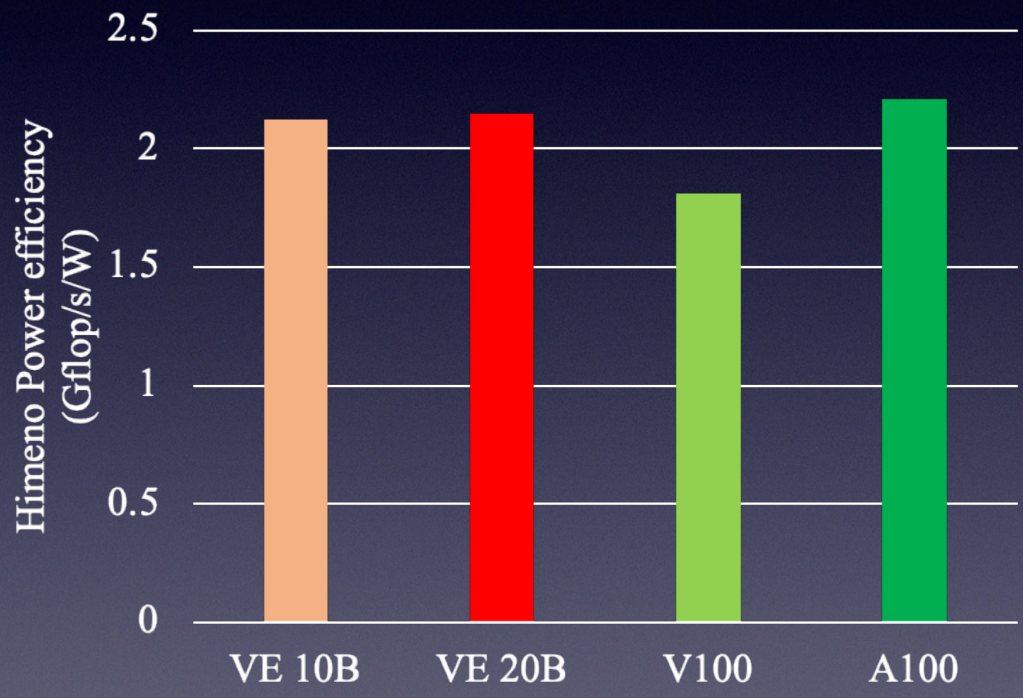
Year	2017	2020	2018	2020	2017	2020
	VE 10B	VE 20B	Xeon 6126	EPYC 7702	V100	A100
Number of cores	8	8	12	64	5120	6912
Peak SP (Tflop/s)	4.30	4.92	1.766	4.096	14	19.5
Peak DP (Tflop/s)	2.15	2.46	0.883	2.048	7	9.7
Memory	6×HBM2	6×HBM2E	6×DDR4	8×DDR4	4×HBM2	6×HBM2E
Mem. BW (GB/s)	1228	1536	128	204.8	900	1555
Mem. Cap. (GB)	48	48	192	256	32	40
LLC BW (TB/s)	2.66	3.00	-	-	2.70	6.88
LLC Cap. (MB)	16	16	19.25	256	6	40



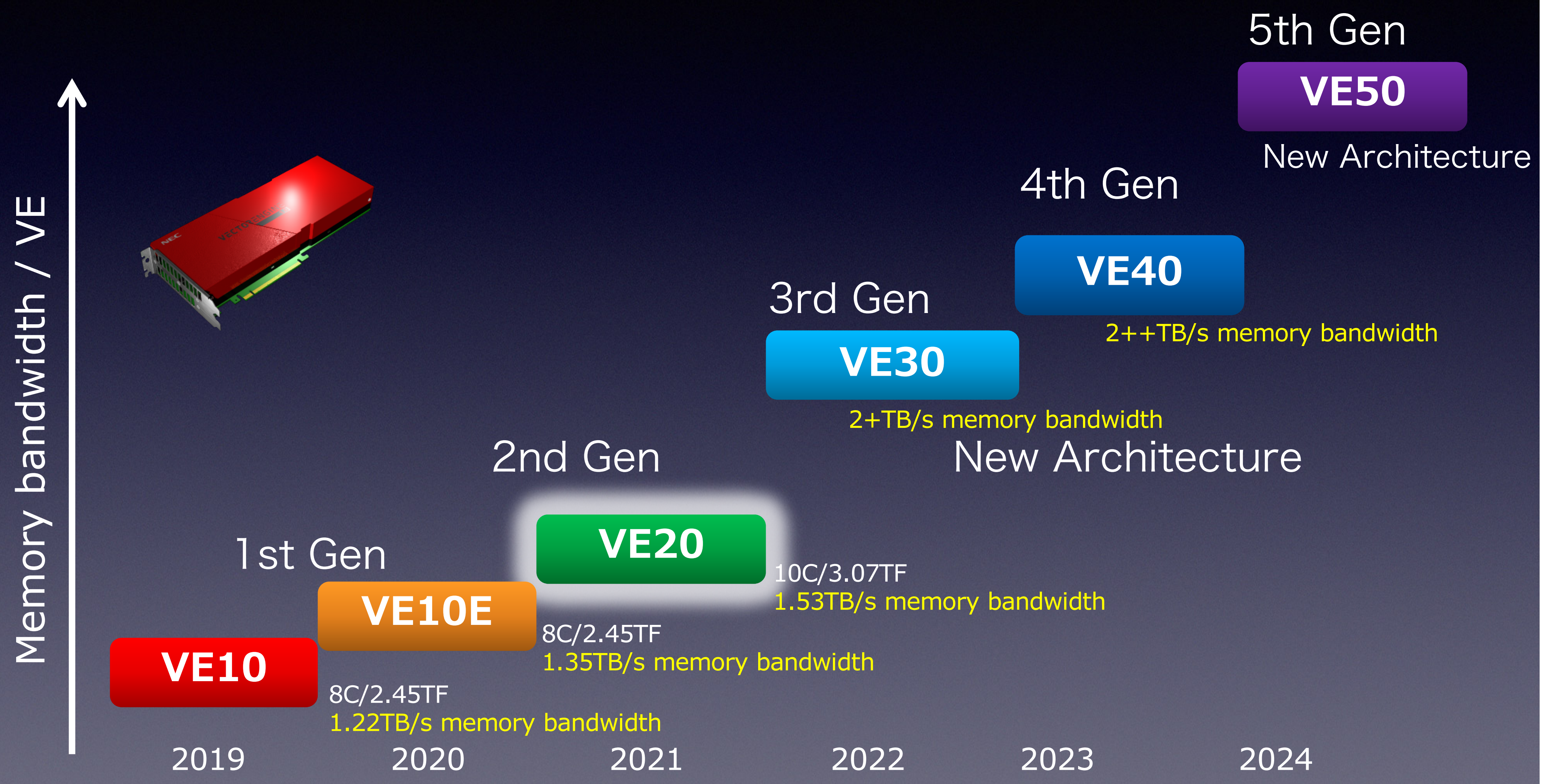


Potentials of SX-Aurora TSUBASA
Power Efficiency

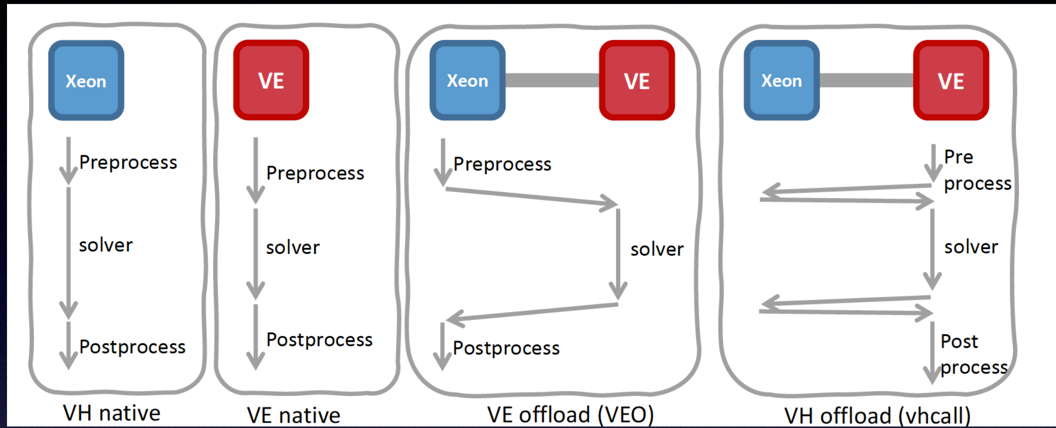


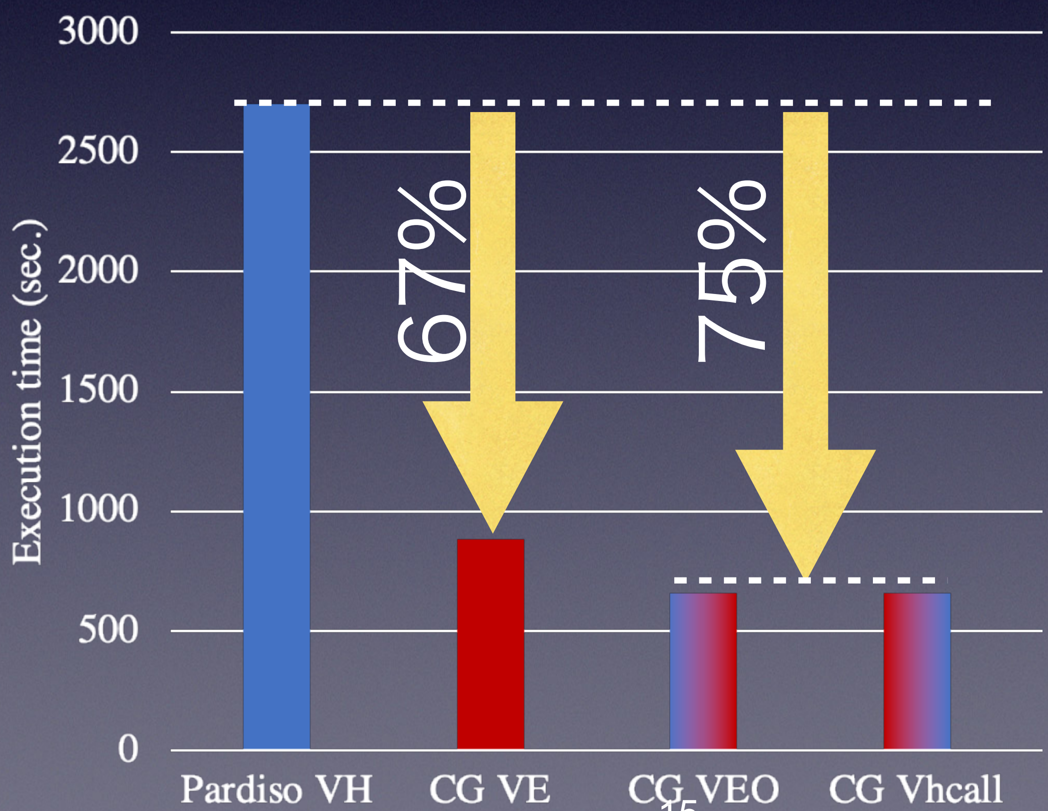


SX-Aurora TSUBASA Tick-Tock Roadmap



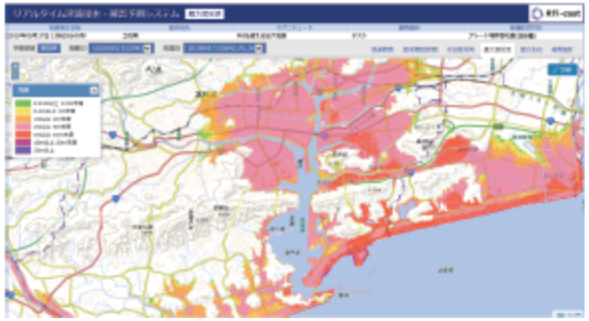
Potentials of SX-Aurora TSUBASA VE-VH Hybrid (Offloading)

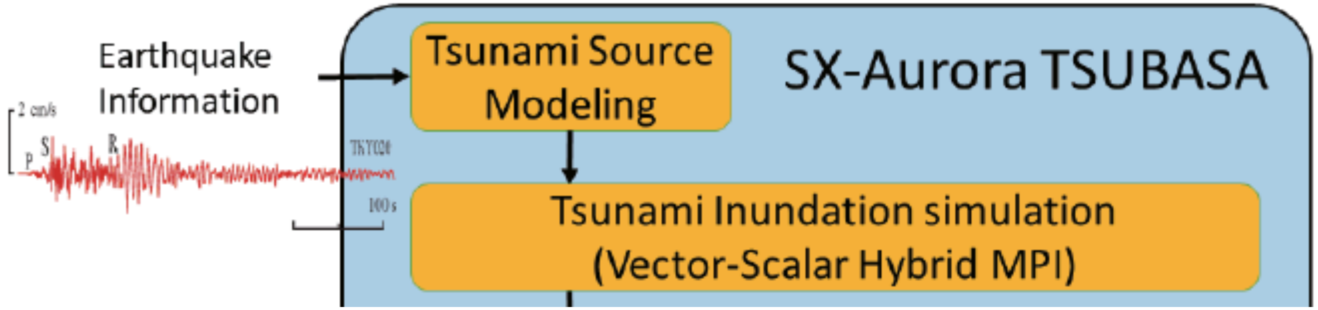


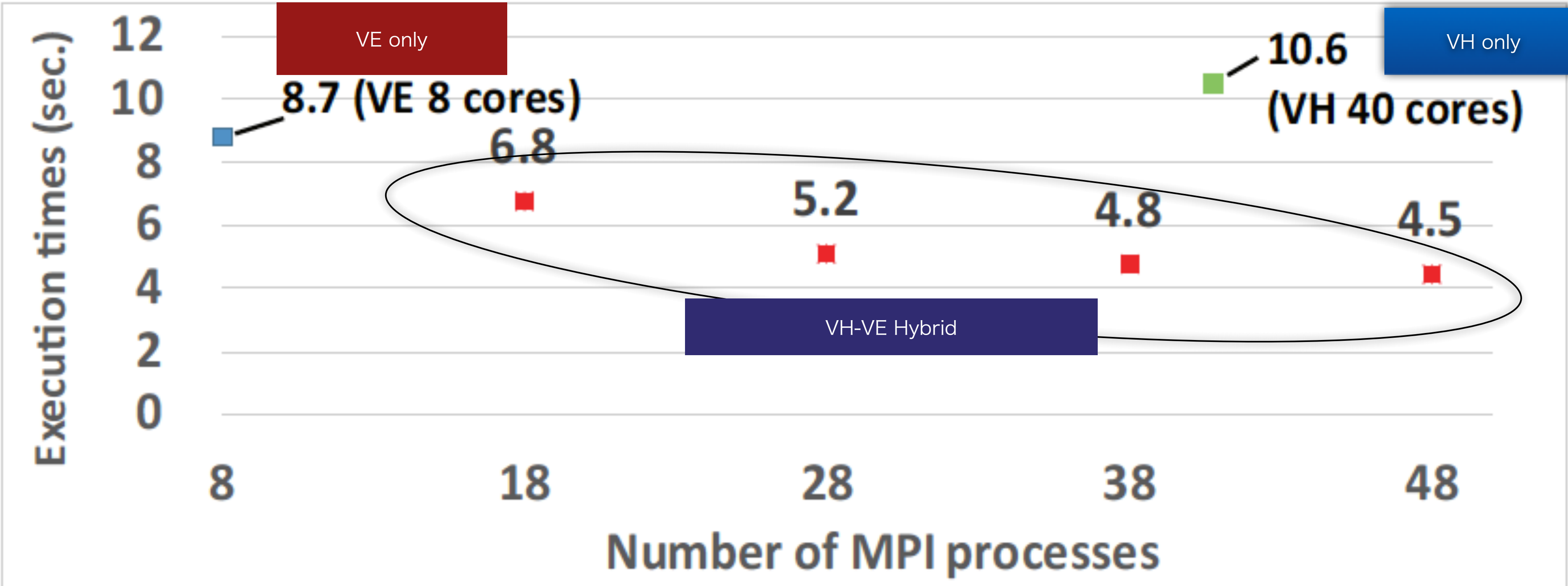


Hiroaki Kobayashi, Tohoku University

Potentials of SX-Aurora TSUBASA VE-VH Hybrid (MPI-Hybrid)







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Hiroaki Kobayashi, Tohoku University

Special Issue on SX-Aurora TSUBASA in Supercomputing Frontiers and Innovations 2021, Vol.8.,No.2.

SUPERCOMPUTING FRONTIERS AND INNOVATIONS

An International Journal

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VOL 8, NO 2 (2021)

DOI: 10.14529/jsfi2102

The special issue on Advance Methods and Technologies on Vector Computing and Data-Processing Using NEC SX-Aurora TSUBASA.

Invited Editors:

- Prof. Hiroaki Kobayashi, Graduate School of Information Sciences, Tohoku University.
- Shintaro Momose, Manager of NEC Corporation, and Visiting Associate Prof. Tohoku University.

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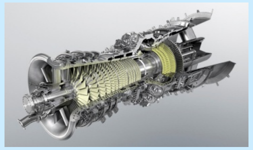
Target Applications Design and Implementation for QA/DA Hybrid on and with SX-Aurora TSUBASA

Hiroaki Kobayashi, Tohoku University

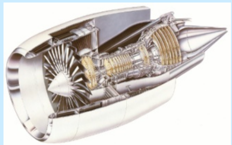
Numerical Turbine: High Performance Turbine Simulator on SX Systems as a Digital Twin of a Real Turbine

Numerical Turbine developed by Prof. Yamamoto of Tohoku University

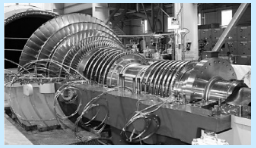
- is a simulation code realizing High-performance and High-reliable Future Turbines and
- has been accelerated on the SX series of Cyberscience Center at Tohoku University.



Gas turbine for plants



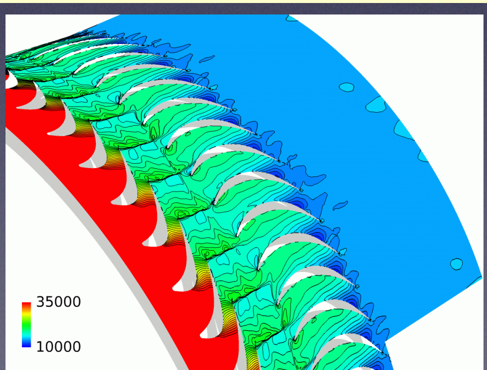
Gas turbine for airplanes



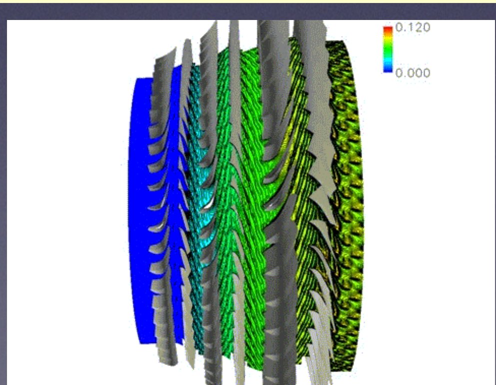
Steam turbine

Only **Numerical Turbine** has achieved the following simulations in the world.

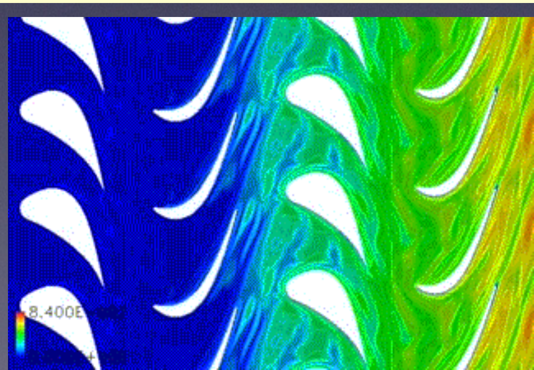
- Unsteady flows with wetness and shocks n actual gas turbines and steam turbines → Resolving such complex flows is crucial for developing high-performance and high-reliable turbines
- Full annulus (maru-goto) simulation for resolving unsteady wet-steam and moist-air flows in actual turbines and compressors



Unsteady shocks generated in turbine stages



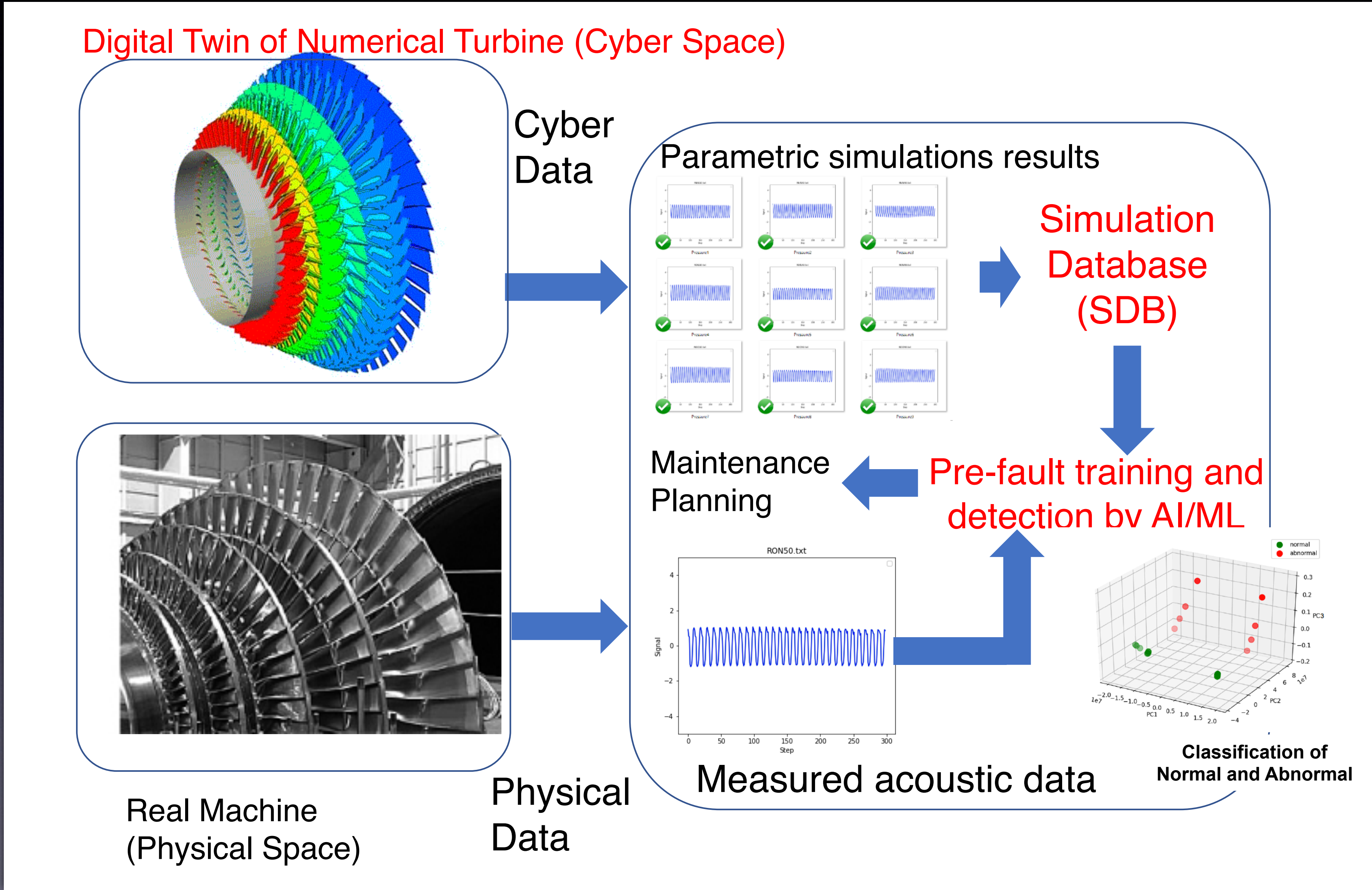
Unsteady wetness in full annulus turbine stages



Unsteady wet-steam flow in turbine stages

Simulation-Driven AI (Simulation-Data for AI)

Target App I: Realization of a Digital Twin of a Real Turbine



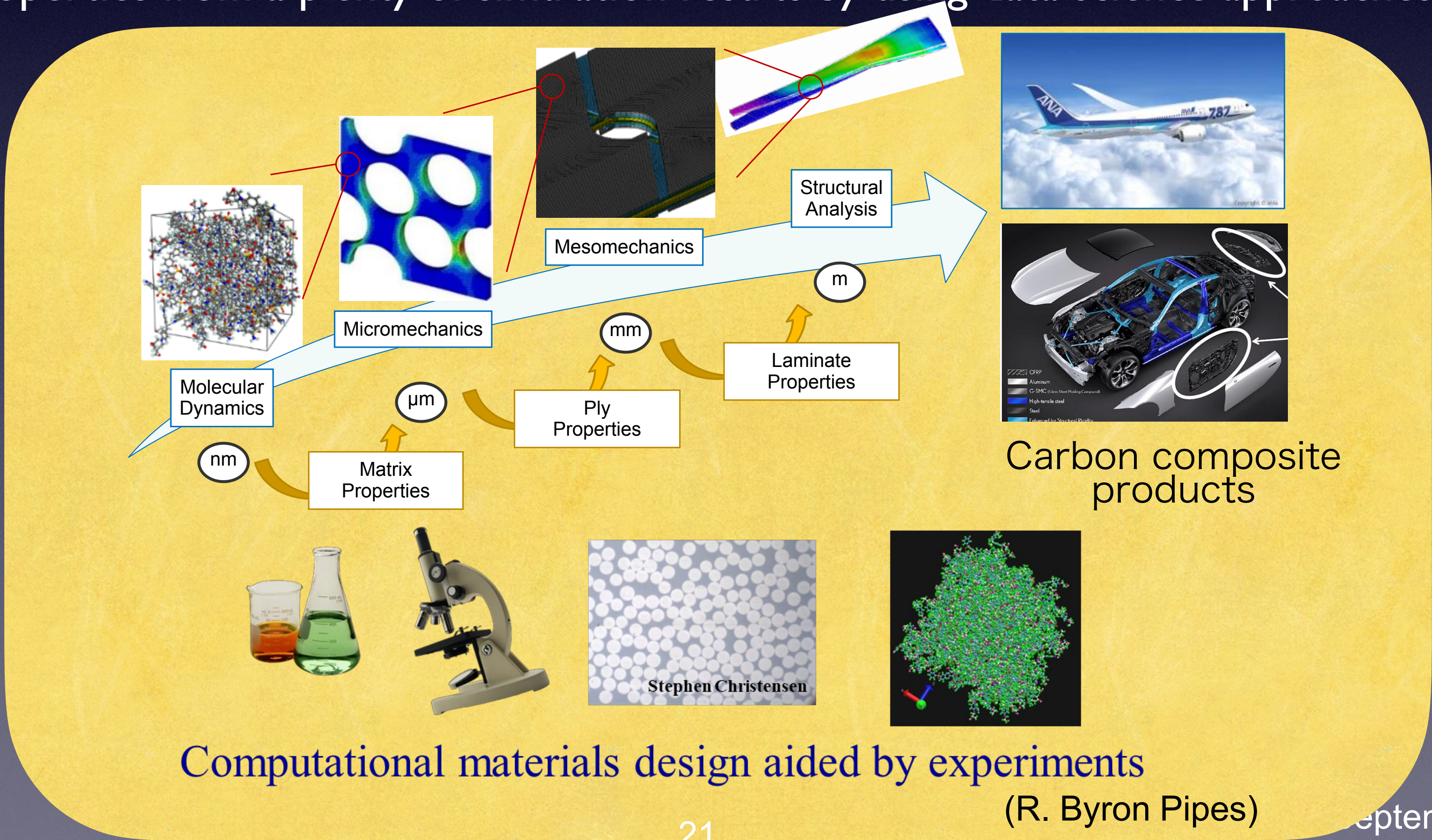
Target App. 2: Materials Integration System R&D

★ Network Polymer (thermoset polymer) is a key material for industrial products with carbon composite

✓ high deformation resistance and high durability to extreme environmental conditions

★ Its design needs high performance simulation, starting from molecular level simulation, up to system level one, such as aircrafts, by using multiscale analysis combined with experiments

✓ Its also needs efficient identification of candidate materials that satisfy the required properties from a plenty of simulation results by using data science approaches



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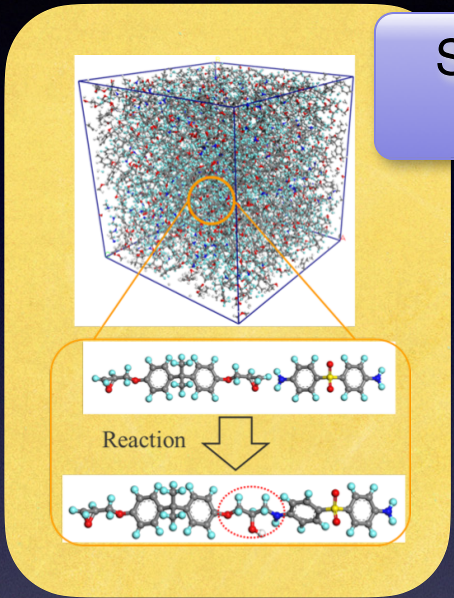
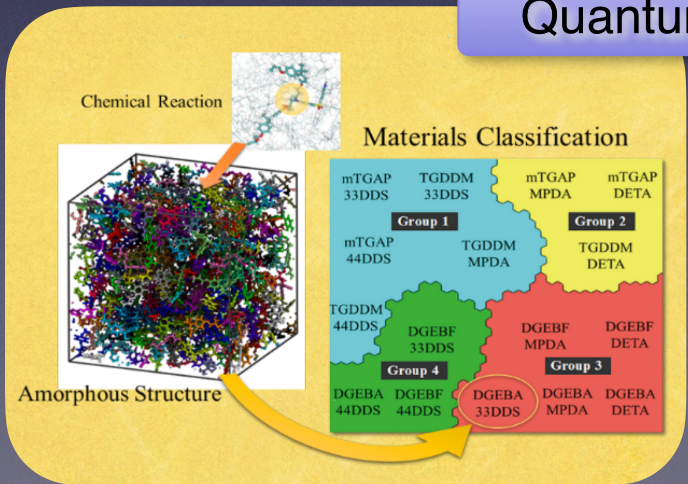
Target App II : QA-Assisted Materials Integration System



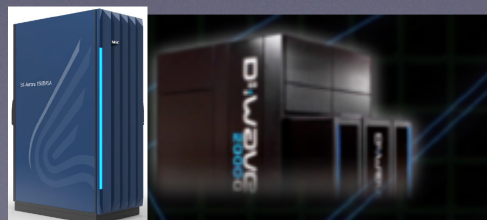
Simulation assisted by next-generation vector-type supercomputing

- ✓More accurate and faster reaction model incorporated into MD simulation for cross-linked network formation in thermosetting resins
- ✓Faster multi-scale simulation for predicting various thermo-mechanical properties

Quantum Annealing-assisted ML frameworks



- ✓Hierarchical screening involving clustering approach
- ✓Highly accurate machine learning model based on polymer physics
- ✓Inverse problem-based optimum design for screening of polymeric materials



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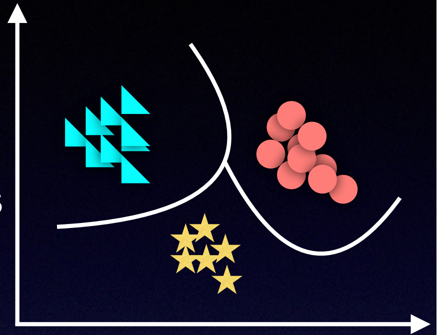
Combinatorial DA Clustering on SX-Aurora TSUBASA
Hybrid Computing of QUBO Generation on VH and Digital Annealing on VE



★ Data Clustering

- ✓ Well-know method to analyze data for data mining such as pattern recognition, image analysis, information retrieval and machine learning as well
- ✓ K-means is popular, but realizes a approximate clustering

★ Combinatorial Clustering

- ✓ precise clustering by considering all the data distances
- ✓ Clustering is defined as a combinatorial optimization problem that can be accelerated by quantum and simulated(digital) annealing.

★ A newly-developed combinatorial clustering for SX-Aurora TSUBASA with digital annealing on VE

- ✓ The one-hot constraint is given separately from the objective function to be minimized, but controlled independently to still keep the one-hot constraint situation.
  - A QUBO is used for definition of the objective function only to have enough precision to represent, resulting in higher clustering quality
- ✓ An Efficient Hybrid Computing of QUBO generation and post-processing of clustering on VH and Digital Annealing on VE

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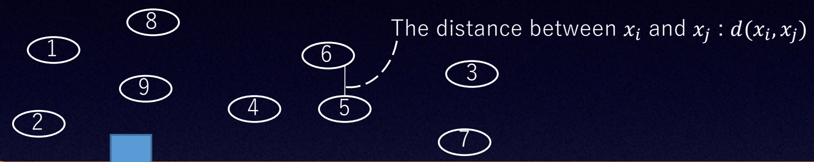
Combinatorial DA Clustering on SX-Aurora TSUBASA
Hybrid Computing of QUBO Generation on VH and Digital Annealing on VE

Pre&Post Processing on VH

① Calculating distances $d(x_i, x_j)$ between all data points



② Generating a QUBO problem with an external constraint

$$\underset{\{q_a^i\}_{i=1\sim N,\ a=1\sim K}}{\operatorname{argmin}} \frac{1}{2} \sum_{i,j=1}^{N} d(x_i, x_j) \sum_{a=1}^{K} q_a^i q_a^j$$

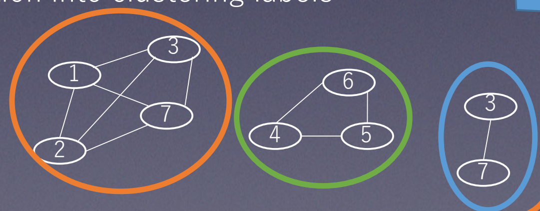
Only one of the variables $q_0^i \sim q_K^i$ being one.

a \ i	1	2	3	4	5	6	7	8	9
1									
2									
3									

- q_a^i expresses whether x_i belongs to a particular cluster a or not.
- The number of ones must be one.
  - One-hot constraint

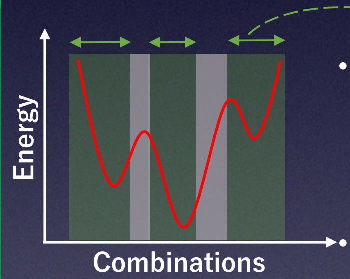
④ Converting the solution into clustering labels

a \ i	1	2	3	4	5	6	7	8	9
a	1	1	3	2	2	2	3	1	1



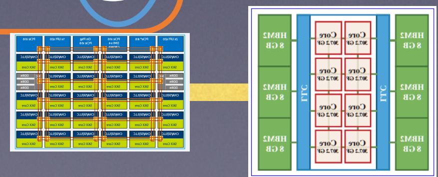
Digital Annealing on VE

③ Searching a solution by SA with an optional setting of an external constraint (SAEC)

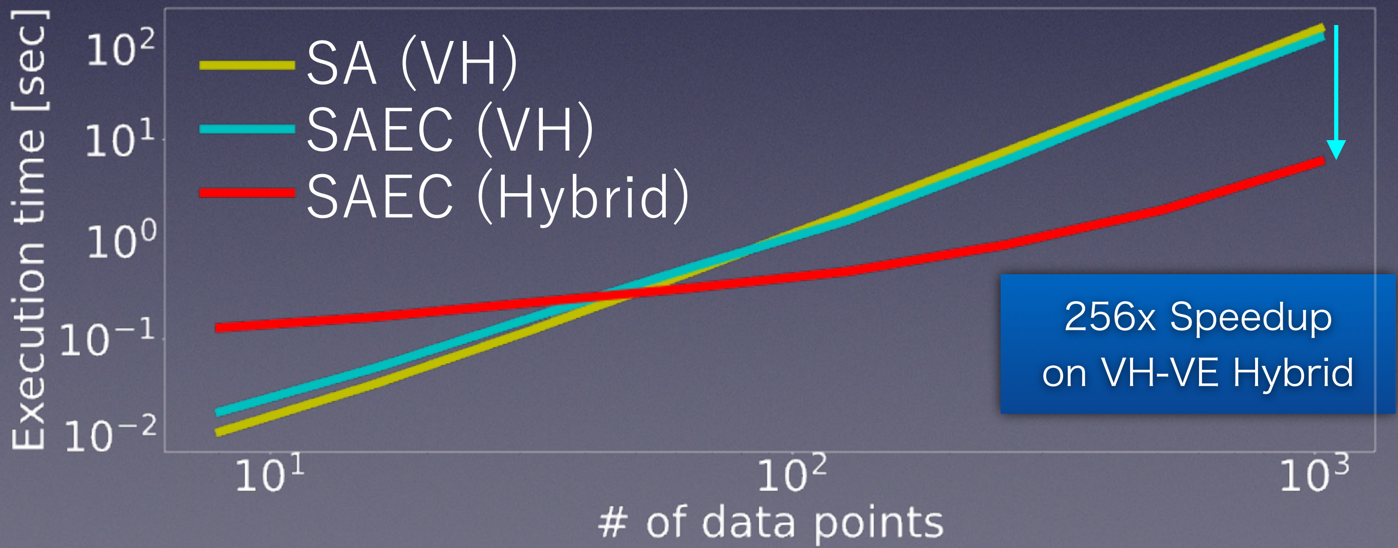


a \ i	1	2	3	4	5	6	7	8	9
1	1	1	0	0	0	0	0	1	1
2	0	0	0	1	1	1	0	0	0
3	0	0	1	0	0	0	1	0	0

- Searching intensively the regions that satisfy the constraint by the bit-flip algorithm.
- The calculation of the energy is a matrix operation and can be accelerated by vector operations.
- The solution satisfying the constraint obtained!



Combinatorial DA Clustering on SX-Aurora TSUBASA
Hybrid Computing of QUBO Generation on VH and Digital Annealing on VE



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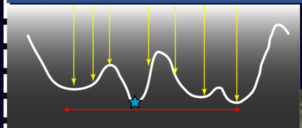
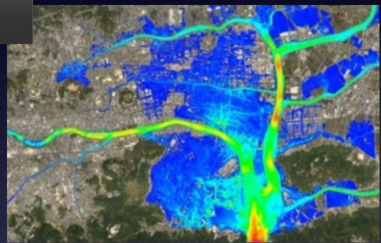
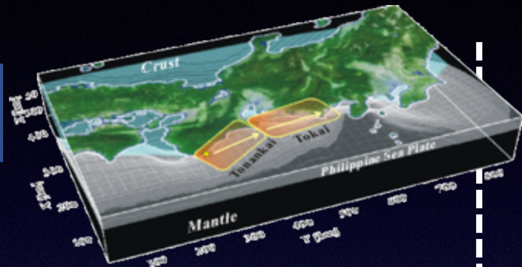
Target Application III:
QA-Enhanced Real-Time Tsunami Inundation Forecasting and Optimal Evacuation Planning

Time

Fault Estimation with QA-enhanced MCMC







Tsunami Inundation Simulation

Optimal Evacuation Planning
with Quantum Annealing

Integrated Programming Framework

D-wave Machine

Aurora TSUBASA Vector Host (Xeon)

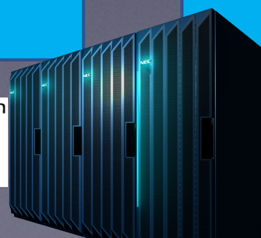
Aurora TSUBASA Vector Engine

Cyberscience Center

Tohoku University -Break limit of your potential- Quantum Annealing Research & Development
QARD
Supported by JST project for creating START

D-Wave The Quantum Computing Company™

Empowered by Innovation NEC



GSIS Graduate School of Information Sciences Tohoku University

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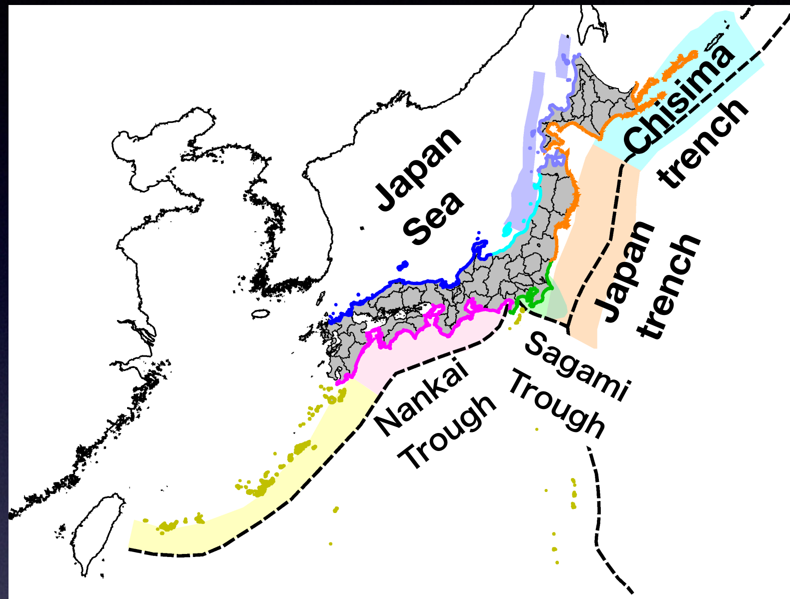
SX-Aurora TSUBASA is a Key Platform for the Full Coverage of Japan in Inundation Damage forecasting

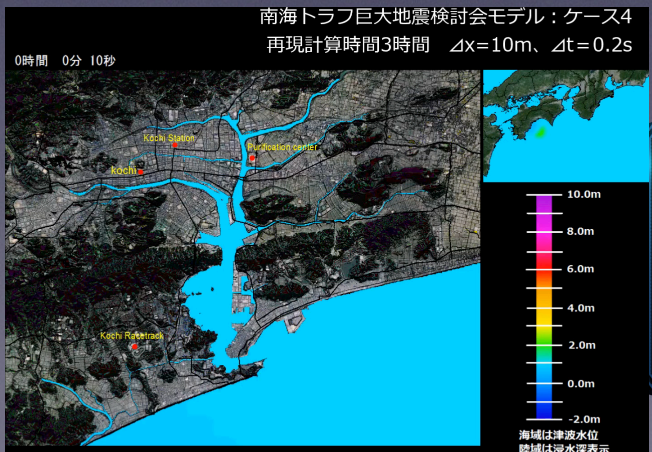


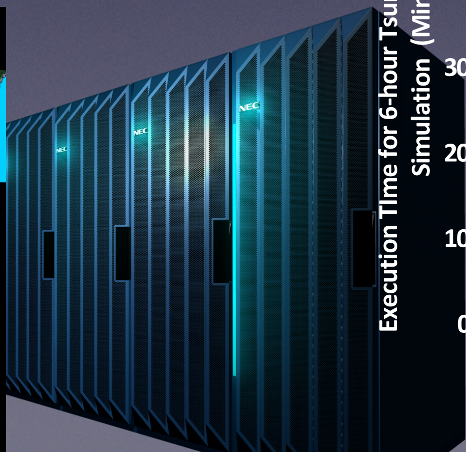
★ **Area Covered**

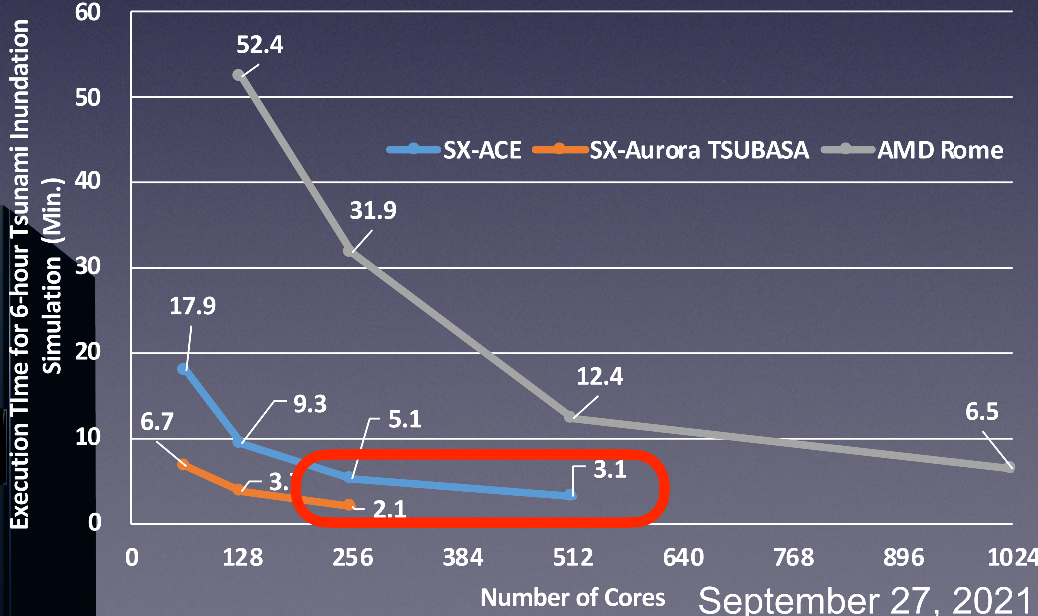
- ✓ From two points (Kochi and Shizuoka areas) to Japan coastal areas along coastlines of 8,000km from Kagoshima up to Ibaraki at a 10mx10m mesh resolution.

★ **Expanding the covered area nation-wide**

- ✓ Up to Hokkaido and then
- ✓ Down to the side of Japan Sea







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Real-Time Evacuation Guidance based on Multi-Agent Simulation Powered by Quantum Annealing

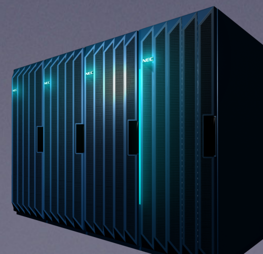
★After the inundation damage estimation is obtained, evaluation guidance to the safety zones will be estimated

- ✓ three candidates for safety evacuation routes obtained by using 1) shortest path algorithm, 2) enforced learning based multi-agent simulation and 3)their combination under the consideration of the inundation damage simulation results,
- ✓ Best evacuation paths are selected based on the locations by using quantum annealing to solve an optimal combinatorial problem to maximize survivors from the inundation

Evacuation on best routing policy

Integrated Programming Framework

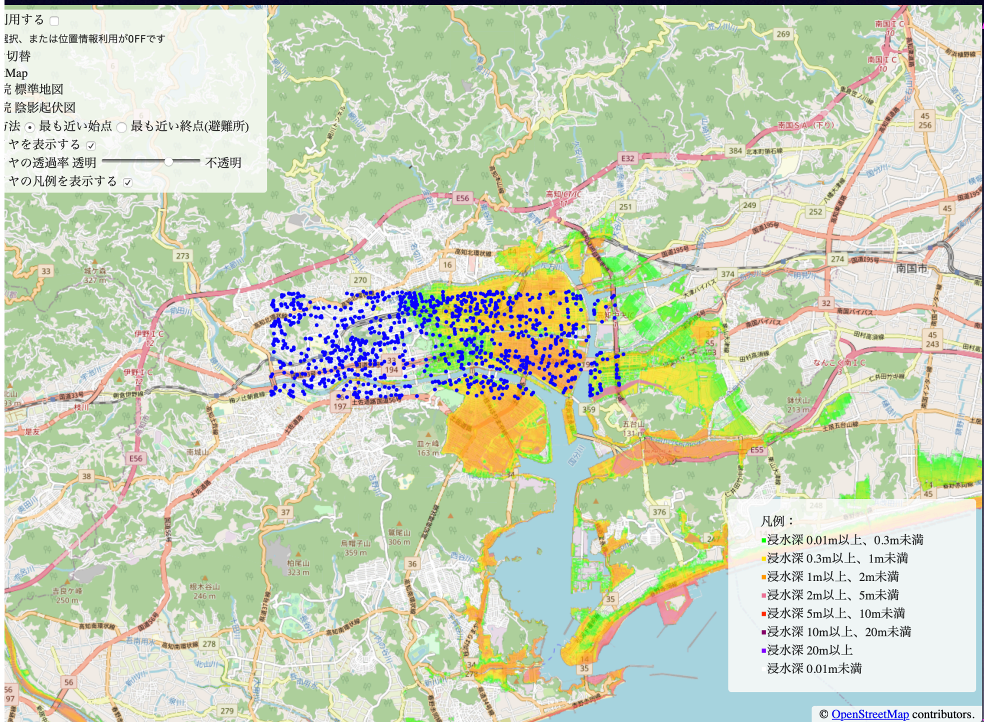
D-wave Machine — Aurora TSUBASA Vector Host (Xeon) — Aurora TSUBASA Vector Engine

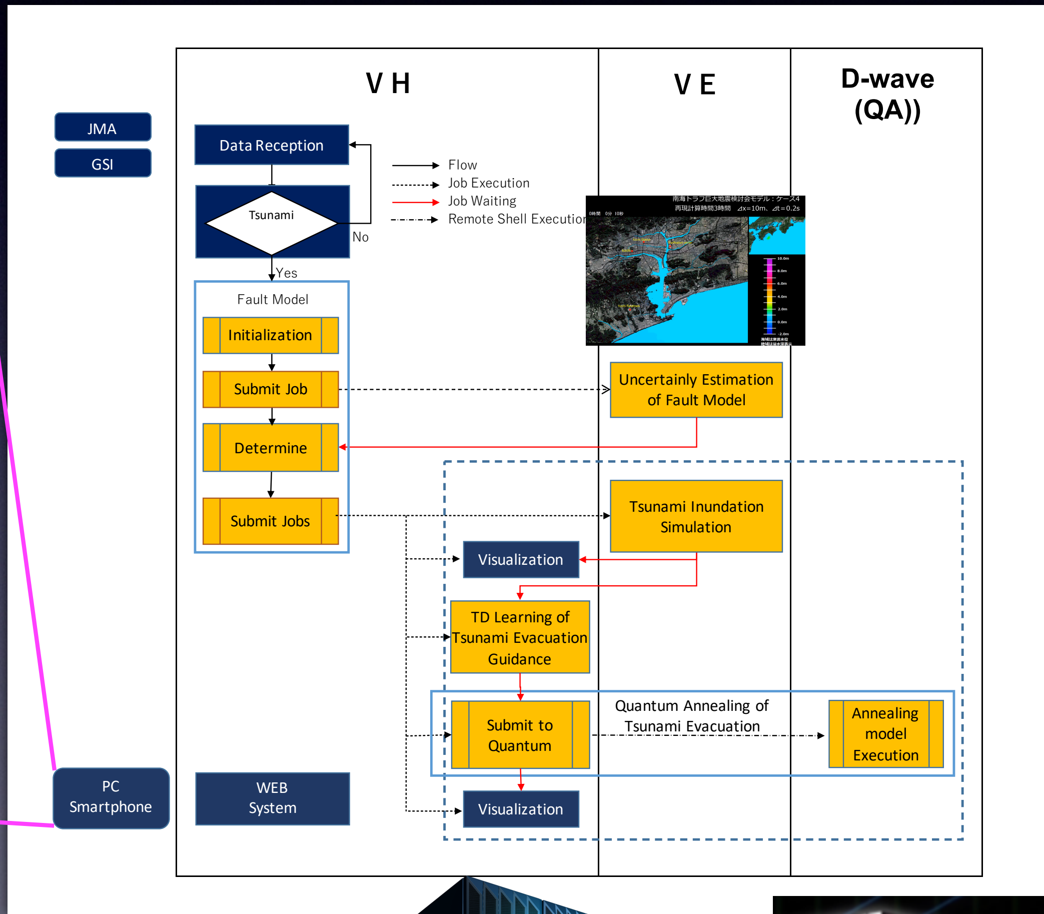


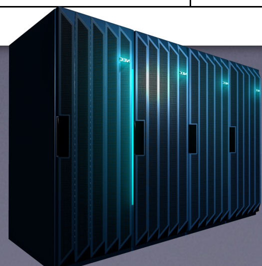
September 27, 2021

A Workflow of QA-Classical HPC Hybrid Computing for TSUNAMI Inundation Simulation and Optimal Evacuation Path Planning

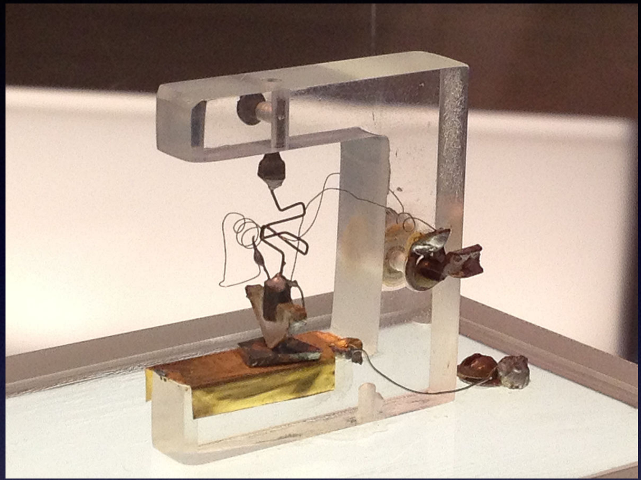
Obtained Optimal Evacuation Path Results in the Case of Kochi City (Demo)



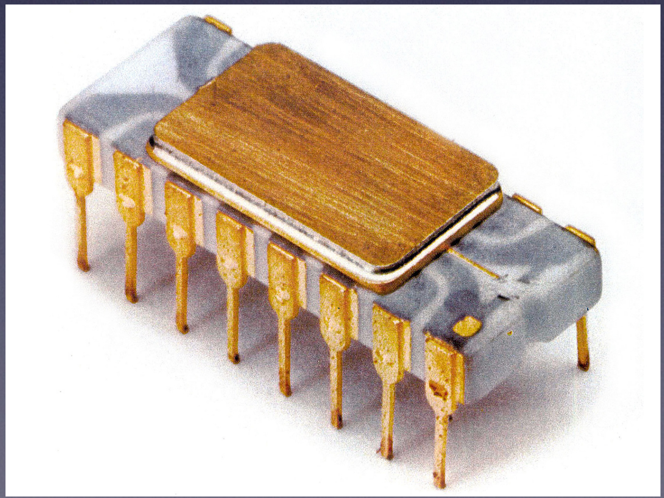




We are seeing The Dawn of Quantum Computing!?



The first transistor ever made, built by John Bardeen, William Shockley and Walter H. Brattain of Bell Labs in 1947.



The Intel 4004 was the world's first microprocessor—
a complete general-purpose CPU on a single chip. Released in March 1971,

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Summary

- Realization of general-purpose computing by ensemble of domain specific architectures as the next generation computing infrastructure toward post Moore's era
  - ✓ Maximize computing performance per cost and/or power best suited for a specific domain
  - ✓ Best mix of domain specific architectures that satisfies the demands of a wide variety of applications
- ★ R&D of a next generation HPC infrastructure: Fusion of Quantum-Annealing and classical HPC in a unified way
  - ✓ SX-Aurora TSUBASA, combination of vector engine and X86 engine, has a great potential to achieve a high sustained performance because of its best mix of vector architecture for memory-intensive apps. and x86 architecture for complicated control-intensive apps.
  - ✓ D-wave machine, A Quantum annealing machine, is the best domain specific architecture for combinatorial problems in the post-Moore era
- ★ R&D of three innovative killer apps:
  - ✓ digital twin of a power generating Turbine for its effective operation and maintenance, and
  - ✓ material informatics for efficient carbon composite products design
  - ✓ real-time optimal Tsunami inundation evaluation planning,
- ★ Quantum annealing has a potential as a game changer toward the post-Moore era, but still is in its infancy
  - ✓ We are seeing The Dawn of Quantum Computing!?
  - ✓ Yes it needs more efforts and breakthrough to make it happen!
  - Digital Annealing on SX-Aurora TSUBASA is reasonable choice until the quantum annealing becomes practical!

Hiroaki Kobayashi, Tohoku University

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